High Frequency Multipurpose SiC MOSFET Driver

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Abstract. *This article describes a new multipurpose Silicone-Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) driver, which was designed and manufactured for a high frequency operating SiC transistor as a semiconductor switching device of power converters. The design of the introduced driver enables to adjust the output voltage levels easily by choosing the integrated linear voltage stabilizers with suitable output parameters used for Printed Circuit Board (PCB) mounting. The voltage insulation of the proposed driver between the primary control side and the secondary output side is performed by MGJ6D12H24MC muRata Ps DC-DC converter with a declared dv/dt immunity 80 kV/1000 ms at 1.6 kV and by IX3180 IXYS High Speed gate driver optocouplers with a declared 10 kV/1000 ms minimum common mode rejection at 1.5 kV. The voltage insulation of these coupling elements is accompanied by safety gaps on the PCB. These insulation features enable the proposed driver to work on high frequencies as a high-side transistor of H-bridges as same as in other power converter topologies with a high frequency and high voltage stress of the insulation border. The proposed driver also provides the possibility of tripping the signal, when the short circuit of the controlled power transistor occurs.*

Keywords

Driver, high switching frequency, MOSFET, multipurpose driver, overshoot, SiC.

1. Introduction

Modern Silicone-Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFET) can be used in power converter applications working with high switching frequencies in a range from tens of kHz up to MHz. High switching frequency with a combination of low transistor switching charge brings a possibility of fast switching with low power losses [1] and [2]. This leads to low switching losses due to fast transistor opening and closing and low consumed power for control the transistor due to low gate charge [3] and [4].

The requirements for a precise gate-source voltage control arise from accomplish the precise switching stated above [5]. Fast rise and fall times of the gate-source voltage are necessary for a fast switching and related low switching loss achievement [6]. The related fast switching enables the converter to work with high control dynamics, which is often required within control algorithms [7]. The steady levels of the gate-source voltage, mainly the positive level of the switched-on state, are demanded to be close to the maximum rating values of the used power transistor to eliminate the conduction and leakage losses [8]. These requirements originate especially in a necessity of precise tune up the driver output resistance in high voltage converter applications. It is caused by the wave impedance of the cable line applied between the driver and controlled transistor and the transistor input capacity [9], [10], and [11]. This adjustment is usually necessary because of the gate-source voltage overshoot originated at the end of the control signal rising edge and the falling edge, respectively. Generally, it is demanded to develop a multipurpose driver adjustable for the specific application.

The high voltage stress of insulation border between the primary and secondary parts of the driver is originated in some applications. That can be seen especially in H-bridges where the power transistor is drain connected to the steady point of power voltage with reference to the control system ground. This voltage stress is more strenuous with a faster switching and higher switched voltage due to capacity current flowing via the insulation border and stressing the isolating dielectric.

In general, relatively high switching frequencies and related fast rise and fall times of switched semiconductors are achievable with the modern MOSFETs. However, it means precisely tune up the driver buffer output resistivity according to the output cable inductance, the MOSFET input capacity, and the related gate-source voltage overshoot. The overshoot is higher with a higher rising and falling gate-source voltage slopes. High switching frequencies of the applications, where the transistor source terminal changes its electric potential with changing the switch state means high insulation border stress. In general, many drivers are commercially available, and many driver designs were already published, see [12], [13], [14], [15], [16], [17], [18], [19], and [20].

The goal of the paper is to present a multipurpose driver concept with a few novel potentials according to the following specific application requirements:

- easy setup of the steady on and off state output voltage levels,
- easy setup of the output resistance to tune it up according to the output cable impedance,
- high dv/dt insulation border immunity up to 1.7 kV·µs^{-1},
- signal trip extension,
- extension of transferring the information about drain-source voltage presence,
- possibility to use the device not as a transistor driver, but as an insulated voltage detector.

All the mentioned features should be feasible by choosing the appropriate PCB assembly. This makes the driver easy to release for a specific application. Moreover, it represses the risk of malfunction of less reliable parts, such as potentiometers. These parts are not used in the proposed concept.

2. Proposed Driver Concept

2.1. General Description

The proposed driver PCB contains 3 ports at the primary side and a group of 3 terminals at the secondary side, each one for one MOSFET pin, see Fig. 1. The first primary port J1 contains the power supply terminals for 9.6–18 V DC with the negative pole connected to the signal ground. This port also contains an input signal for driving the controlled transistor and it is ready to trace the controlled transistor short circuit detection trip signal too.

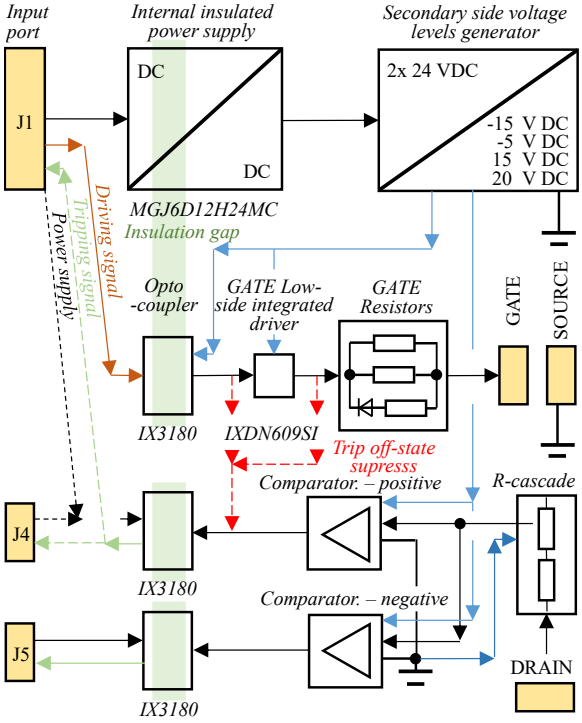

Fig. 1: Proposed driver simplified block diagram.

The next 2 primary ports contain output signals of the secondary drain-source voltage detections, port J4 reacts on positive voltage, port J5 on negative. Each of these ports has an independent power supply on the primary side, which is galvanically insulated. It can work with different voltage signal state levels according to the connected system, the voltage adjustment is possible within the choice of PCB mounting combination.

It is also possible to negate the output signal at the primary side of the positive drain-source voltage detection, which can be beneficial mainly if this signal is used as a trip function. The positive drain-source voltage detector output can be traced in the port J1 with a common signal ground as same as in port J4 with an independent ground system. In general, the positive drain-source voltage detection can be used

as a trip function - in this case, the detector output is suppressed when the output transistor is in an off state. This is performed to avoid the false fault detection caused by the presence of detected voltage on the switched-off semiconductor. If the suppression is not performed, the detector output just follows the detected voltage.

2.2. Secondary Side Power Supply System

The proposed concept contains a DC-DC MGJ6D12H24MC muRata Ps auxiliary source which provides the high du/dt immunity galvanic insulation of the power supply system. The unit of secondary side power supply stabilization generates 4 voltage levels, which are assumed to −15 V, −5 V, +15 V and +20 V, as defaults.

The levels +/−15 V are traced onto power supplies of fast operational amplifiers, which are used as comparators within the units of drain-source voltage detections, if these functions are released. The secondary side of the driving signal optocoupler power supply is supplied asymmetrically, +15 V/−5 V, so the level +15 V is also used there. There is currently no expectation of demand to change the +/−15 V values, but it could be demanded, e.g. in the case of the used operational amplifiers change. In this case, it can be adjusted by changing the related reference resistors series near the linear voltage regulators or by changing these regulators, which are used in the TO-252-3 and SOT-89 package, respectively. If the drain-source voltage detections are not used, PCB mounting the −15 V regulator is not necessary.

The default levels assumed as −5 V, +20 V are used as voltages, which are switched at the gate output. These should be set according to the applied power transistor on- and off-state nominal voltage levels and the overshoot of the gate-source voltage on the applied transistor at the end of the transient switching processes.

These voltage levels are generated by the linear voltage regulators with no reference resistors and with the signal ground connected directly to the secondary ground. This ground is also connected to the transistor source potential.

The voltage regulators are used in the TO-252 package and belong to the well-known LM78xx and LM79xx series, respectively. It is necessary to set these voltage levels by choosing the appropriate voltage regulators.

The nominal off and on-state power MOSFET transistors gate-source voltages are usually asymmetrical with a lower negative level. Because of that, the secondary ground connected to the output transistor source is not connected to the middle of the DC-DC insulation auxiliary source output, even though these 2 × 24 V DC outputs are connected in series.

The secondary side ground is connected to the output of another −5 V DC linear voltage regulator, which moves the reference ground from the middle of 2 × 24 V about 5 V down. This ensures that there are available c. +29 V and −9 V as the inputs for the steady state gate-source voltage regulators.

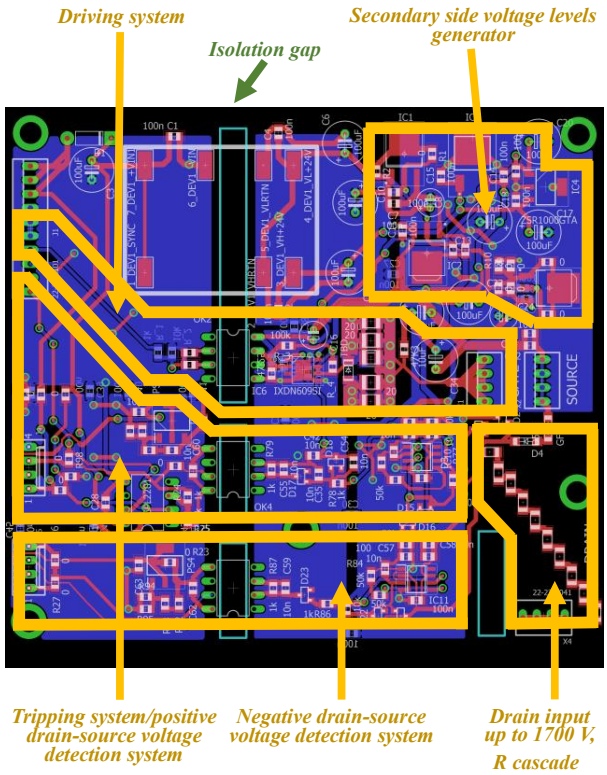

Fig. 2: Proposed driver PCB design layout, Eagle export, blue color - bottom vias, red color - top vias.

2.3. Driving System

The driving system contains the cascaded optocoupler IX3180, an integrated low-side MOSFET driver IXDN609SI and resistive buffer for parallel package 1210 resistors. Fast rectifying bypass diode for coupling the parallel resistors with other resistors for the negative output voltage is also installed.

The mentioned elements also contain an output to suppress the trip output to do not signalize the fail, when the power transistor is in the off-state. It is not necessary to mount parts of all the output resistors PCB pads. However, it is important to tune the total value according to the applied MOSFET and the line cable between the power transistor and the driver output [9]. It is also important to find an optimal resistors combination according to the power loss limitation of these elements.

2.4. Tripping System/D-S Voltage Detection

The tripping system/positive D-S voltage detector is based on the input R-cascade 10×1206 package. This cascade couples the DRAIN input terminal, see Fig. 1, with a pair of diodes in anti-series, which ground the R-cascade via SOURCE terminal, see Fig. 1. The anti-series diodes limit the voltage between the output of the R-cascade and the system ground. This voltage is traced to comparator based on operational amplifier ADA4627. The comparison reference must be set by the related pair of resistors. The proposed PCB layout of the comparator output contains pads for placing the resistor and the capacitor for the low pass filtering at the comparator output.

The input R-cascade also originates the RC low pass filter together with diodes PN-junctions parasitic capacities. Choice of an optimal combination of input resistivity and the grounding diodes then can be used for filtering the input signal.

The main feature of the proposed positive D-S voltage detector system is the possibility of tuning up the sensitivity within a few levels. Firstly, the low pass filter originated by the input R-cascade and the related diodes can be used to suppress the noise received by the operational amplifier. Secondly, the low-pass filter, originated by the RC element of R_1 and C_1, can be used to suppress some fast transient peaks at the operational amplifier output, see Fig. 3.

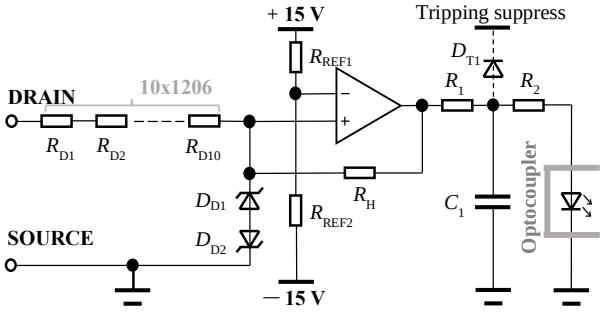

Fig. 3: Tripping system/positive D-S voltage detector system simplified circuit diagram.

Setting up the reference resistors R_{REF1} and R_{REF2} affects the reference comparison level and the input signal-to-noise ratio too.

3. Proposed Driver Prototype

The driver prototype was realized for driving SiC C2M0045170D MOSFET manufactured by CREE, Inc. The output resistivity was set to approximately 3.33 Ω for positive G-S voltage and 2.22 Ω for negative voltage, using 9×20 Ω resistors. The steady positive output voltage was set to +20 V, the steady negative output voltage was set to −5 V.

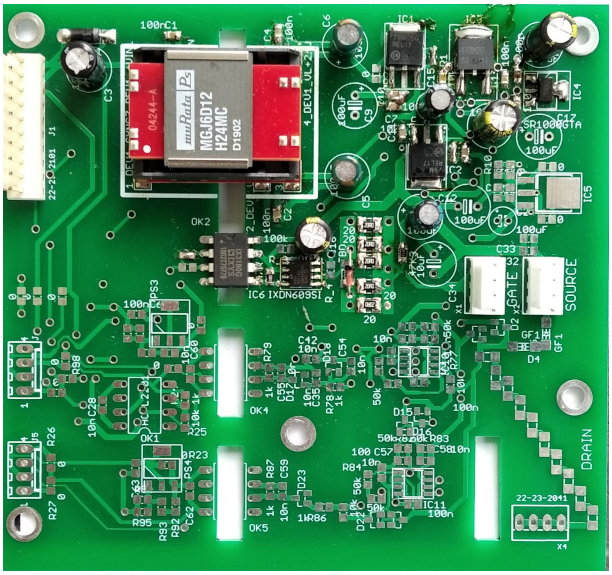

Fig. 4: Mounted proposed driver PCB.

4. Obtained Results

The proposed driver was applied for test onto Step-down converter based on the stated C2M0045170D MOSFET using up to 1000 V switched voltage and with the interconnection of the power transistor to the proposed driver via coaxial approximately 20 cm long cable.

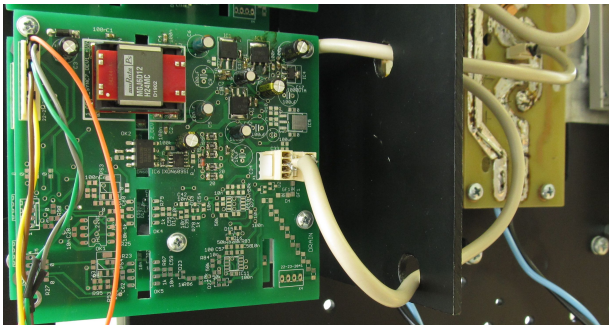

Fig. 5: Tested driver prototype application.

In Fig. 7 and Fig. 8, the responses obtained within the first driver test are presented. The test was performed without voltage at the power circuit. The switching frequency up to 500 kHz was achieved, ordinary voltage scope probes were used.

The obtained turn-on delay was approx. 150 ns and turn - off delay was approx. 220 ns, see Fig. 8. The low overshoots can be seen within the reached gate-source voltage curve, see Fig. 7 and Fig. 8.

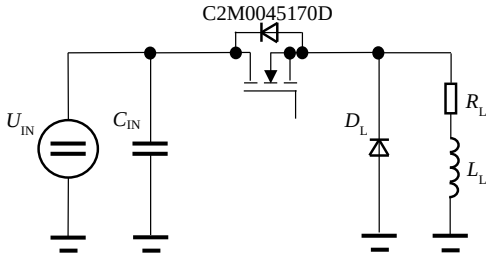

Fig. 6: Testing power circuit diagram.

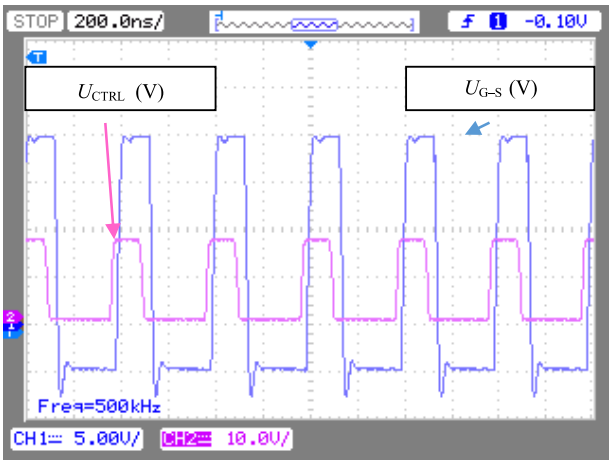

Fig. 7: Driver prototype response, no voltage at the power circuit, input driver signal voltage 1:1 (V) - violet curve, reached G-S voltage directly on the power transistor 1:1 (V) - blue curve.

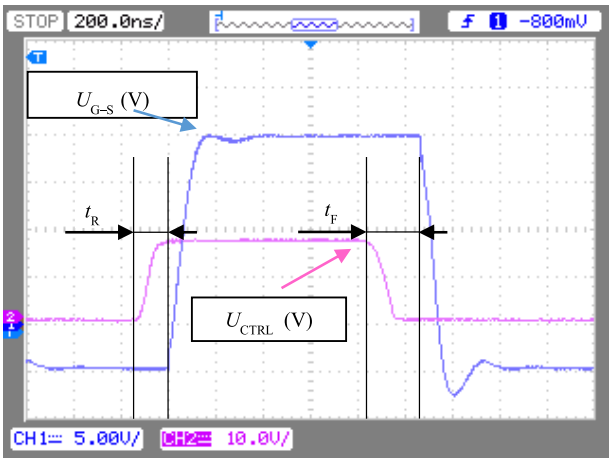

Fig. 8: Detailed driver prototype response, no voltage at the power circuit, input driver signal voltage 1:1 (V) - violet curve, reached G-S voltage directly on the power transistor 1:1 (V) - blue curve.

It is important not to exceed the switched MOSFET absolute maximum rating, which is passed, but the final overshoots are different because of the reverse transfer capacitance impact, see Fig. 12 and Fig. 13.

The responses measured via the probes mentioned in App. A and App. B are shown in Fig. 9, Fig. 10, Fig. 11, Fig. 12, and Fig. 13. The nominal output capacitance of the used C2M0045170D MOSFET is 171 pF. The nominal voltage probe input capacity is less than 5.5 pF (the drain connected voltage probe input terminal is not connected to the floating voltage potential, so there is no input capacity impact). As can be seen, the connected voltage probe input capacity is much lower than the MOSFET output capacity, so the minimal impact onto the measured transient state can be supposed.

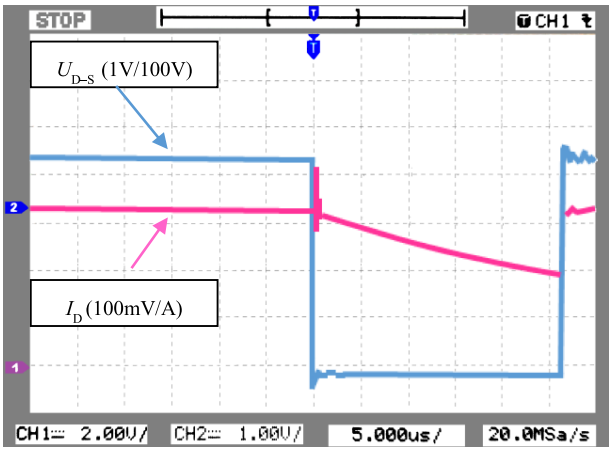

Fig. 9: Obtained one-pulse switching process at $U_{IN} = 1000$ V, drain-source voltage 1:100 (V) - blue curve, drain current 100 mV/A (V) - violet curve.

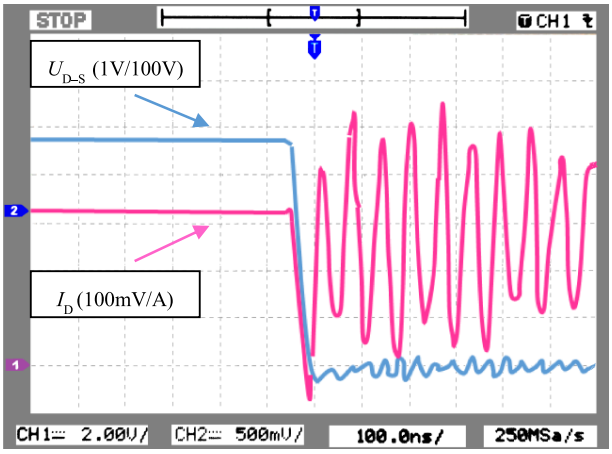

Fig. 10: Obtained switching-on process detail at $U_{IN} = 1000$ V - drain-source voltage 1:100 (V) - blue curve, drain current 100 mV/A (V) - violet curve.

The proposed prototype was tested via one-pulse, which occurred for 25 µs. The switching pulse process can be seen in Fig. 9, where the drain-source voltage falls down at the beginning of the switching-on process, and the drain current flowing through the *RL* load begins exponentially growing up at the same time. This is in progress until the beginning of the switching-off process, when the drain current falls down to zero and the drain-source voltage grows to U_{IN} value over the switching-off overshoot.

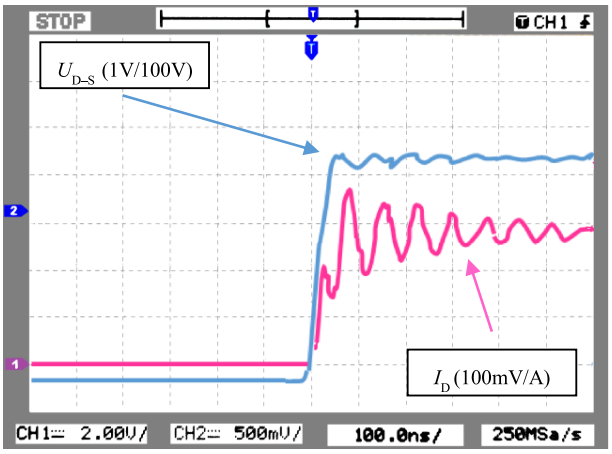

Fig. 11: Obtained switching off process detail at $U_{IN} = 1000$ V - drain-source voltage 1:100 (V) - blue curve, drain current 100 mV/A (V) - violet curve.

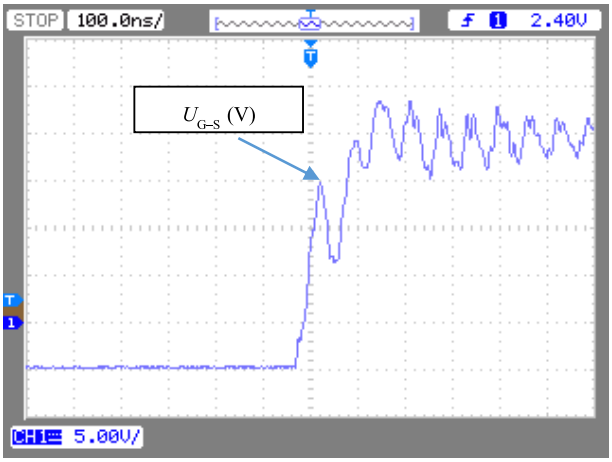

Fig. 12: Obtained switching on process detail at $U_{IN} = 1000$ V - gate-source voltage measured directly on power transistor (V).

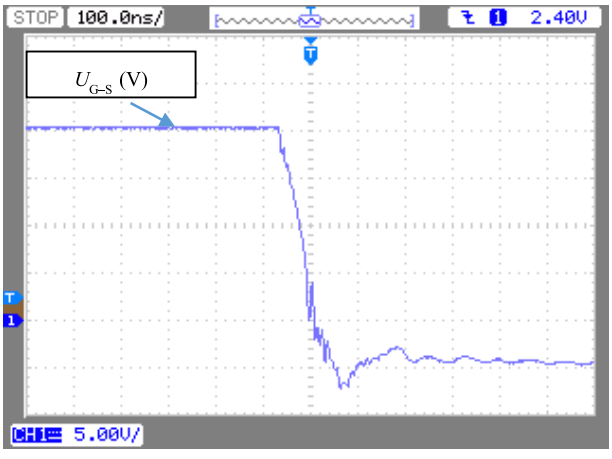

Fig. 13: Obtained switching off process detail at $U_{IN} = 1000$ V, gate-source voltage measured directly on power transistor (V).

The highly smoothed quasi-periodic multi-harmonics drain current oscillations can be observed within the scoped curves, see Fig. 10 and Fig. 11, which represent the details of the switching-on and switching-off processes. These oscillations are caused by a parasitic LC circuit generated by the inductance of the wires between the power MOSFET source and the load and by the P-N junction capacity of the load diode D_L (see Fig. 6).

However, the drain current oscillates shortly after the switching-on process is over, but the power transistor perfectly switches-on with no oscillations within the switching process. It can be seen in Fig. 10 from the curve of the drain-source voltage, which oscillates slightly near the steady state voltage drop value.

The obtained rise time in Fig. 10 is approx. 40 ns, which is close to the nominal value of 20 ns. The nominal turn-on delay is 65 ns. The used voltage probe rise time is less than 14 ns, which demonstrates the possibility of monitoring this curve correctly by the probe.

The drain current quasi-periodic oscillations can be also observed at the switching off-process, see Fig. 11, but the drain-source voltage curve rises continuously, within 20 ns, which is close to the nominal fall time of 18 ns.

Figure 12 and Fig. 13 show the gate-source voltage measured within the same switching-on and switching-off process, respectively, as it is reflected within Fig. 10 and Fig. 11. Some transpositions of the drain current oscillations to the gate-source voltage, can be observed there, see Fig. 12 and Fig. 13.

However, the overshoot of the rising slope does not exceed 25 V, which is the applied MOSFET absolute maximum rating, see Fig. 12.

The falling slope within the switching-off process does not exceed −10 V, which is the used MOSFET absolute maximum rating, see Fig. 13.

5. Conclusion

A new SiC MOSFET driver is presented in the paper. It was discovered that the tuned up realized driver prototype is able to rich the nominal values of rise and fall times of the assigned controlled power transistor, even though there was no effort to localize the driver as close as possible to the controlled transistor. The approx. 20 cm long coaxial cable was used in this case. Despite the related wire inductance, the used MOSFET gate-source voltage absolute maximum ratings were not exceeded. The steady states gate-source voltages were set to the transistor recommended values.

The obtained results are very beneficial from the practical point of view, because it is not usually possible to locate the driver absolutely

near the driven power transistor according to the converter construction aspects. The proposed solution enables to work near the transistor limits and also with the use of a cable between the driver and the power transistor.

The suppressed current oscillations can be observed at the ends of the switching processes. These are originated by the response of the parasitic *LC* element of the testing circuit. Although these oscillations are transferred onto gate-source voltage, the switching processes are continuous, which can be seen from the curves of the drain-source voltage.

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Author Contributions

J.S. and V.D. created the conceptualization and formulated the main ideas of the proposed device including the application requirements leading to the main goals. M.S. and D.K. prepared the prototype design and worked cooperating with V.D. within the prototype building-up process. J.B. and M.S. performed testing and final tunning up the prototype to get the presented obtained results. D.K. and J.B. performed the state of the art investigation and J.S. performed the critical verification of the obtained results and wrote the paper draft iáncluding the original draft preparation, and editing.

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Appendix A Used Drain Current Probe

LEM PR50

- Bandwidth $f_{BW} = 50$ MHz.
- Rise time $t_r < 7$ ns.
- Delay time $t_d < 25$ ns.

Appendix B Used Drain-Source Voltage Probe

Teledyne LeCroy AP031

- Bandwidth $f_{BW} = 25$ MHz.
- Rise time $t_r < 14$ ns.
- Input capacitance $t_d < 5.5$ pF each input terminal to ground.